

REMARKS/ARGUMENTS

Favorable reconsideration of this application is respectfully requested.

Claims 25-34 are pending for examination in this application. Claims 25, 27, 29, 33 and 34 are amended to better clarify the extraction of current through the current sense emitter separate from the main emitter without the introduction of any new matter.

The outstanding Action presents an improper request for formal drawings already submitted in the Office Action Summary Sheet that misstates the pending claims as 23-34 instead of 25-34, a rejection of Claims 25-33 under 35 U.S.C. § 103(a) as being unpatentable over Yanagisawa et al (U.S. Patent No. 5,874,750, Yanagisawa) in view of Takeda et al (1998 International Symposium article, Takeda) and a rejection of Claim 34 under 35 U.S.C. § 103(a) as being unpatentable over Yanagisawa in view of Takeda in further view of Horiguchi et al (U.S. Patent No. 5,910,675).

Turning to the rejection of Claims 25-33, the outstanding Action continues to mistakenly assert that Yanagisawa teaches an injection enhanced gate transistor (IEGT) having a main emitter and a current sense emitter. As has been repeatedly pointed out, even a cursory reading of Yanagisawa reveals that the teachings thereof relate to an insulated gate bipolar transistor (IGBT), not an IEGT. As was further specifically noted in the last response, the IGBT of Yanagisawa has an emitter electrode plate 16 and a collector electrode plate to form a pressure-contact type IGBT which comprises a single-emitter structure and an emitter sensing terminal ES directly connected with the single emitter for monitoring the emitter voltage (which is a potential difference between the emitter on the IGBT chip and the ground of the gate circuit), so that the emitter sensing terminal is not influenced by inductance between the signal emitter and the emitter sensing terminal. Thus, in view of this need for an electrical connection to permit this monitoring of the emitter voltage, the previous response pointed out that could be “no question that the IGBT of Yanagisawa has a single

main emitter and no separate current sense emitter unlike the IEGT of independent Claims 25, 27, 29, 31, and 33.”

The last response went on to point out that the “symbol of an IGBT is shown in the broken line circle in FIG. 8 of Yanagisawa that clearly shows the emitter to which the emitter voltage sensing terminal ES is connected.” It was further pointed out that an “IEGT has two separate emitters, and a symbol thereof is shown in FIG. 24 of the present application in which a main emitter of the IEGT chip 42a is connected to the emitter press-contacting electrode plate 47 via the inductance 53a (see the specification at page 42, lines 14-16, for example), and a sense-side emitter of the IEGT chip 42a is connected to the gate of a transistor Tr and one terminal of a resistor Rs (see the specification at page 42, lines 23-25, for example).” Furthermore, the last response noted it to be “commonly known in the art that the main emitter and sense emitter are separately and isolatedly formed in an IEGT chip and the symbol thereof is shown in FIG. 24 (see page 42, lines 7-9 of the specification, for example)” (emphasis added). The clear thrust of these arguments was the lack of any reasonable disclosure as to any separation in an electrical sense as between the emitter sensing terminal ES and the “directly connected” main emitter of Yanagisawa. Instead of giving the term “separated” this reasonable interpretation and answering the clear intent to define the electrical separation inherent in the claimed “IEGT” with a current sense emitter, the outstanding Action has emphasized the showing of FIG. 6 and col. 5, lines 52-54 that explain a separation exists between an “emitter region” 38 and the emitter electrode 12a. However, the separation between the emitter region 38 and the emitter electrode 12a of Yanagisawa was and is not relevant to the limitation of independent Claims 25, 27, 29, 31, and 33 that recited a “main emitter” that not only has to be electrically connected to a “plate-like emitter press contacting electrode,” this connection has to be the result of the main emitter being pressed by this plate-like emitter press contacting electrode. Accordingly, the

attempt to equate the emitter region 38 of Yanagisawa to the claimed “main emitter” and to emphasize the physical separation illustrated in FIG. 6 and noted at col. 5, lines 52-54, as being between 12a and 38 is without merit.

In any event, to the extent that emitter electrode 12 was intended to be read as the element disclosed by Yanagisawa that could be said to be the main emitter the electrical and physical connection between 12 and 12a is clear from FIG. 6 and col. 5, lines 59-51. moreover, as further noted in the last response, col. 1, lines 62-65 of Yanagisawa disclose an emitter voltage sensing terminal is needed to sense (monitor) voltage of an emitter electrode of the IGBT. Clearly, if the emitter voltage sensing terminal is to sense (monitor) the voltage potential of the emitter electrode of the IGBT, this can only mean that the emitter voltage sensing terminal must be electrically connected directly to the emitter electrode which is connected to the emitter region of the IGBT. As further shown in FIG. 7 of Yanagisawa, the emitter electrode 12 is connected to the emitter region 38 and the emitter sensing electrode 12a is connected to the emitter voltage sensing terminal ES. The emitter electrode 12 and the emitter voltage sensing terminal ES are shown part in FIG. 7, however, these elements are commonly formed by a single emitter electrode 37 as shown in FIG. 6 (see col. 5, lines 29-32 of Yanagisawa).

In other words, the emitter voltage sensing terminal of the IGBT taught by Yanagisawa is to be connected directly to the emitter electrode so as to sense the emitter voltage. If the sensing terminal is connected to a portion separated from the emitter electrode, the correct emitter voltage cannot be detected. To emphasize that the separation required is an electrical one as between the current sense emitter and the main emitter, independent Claims 25, 27, 29, 31, and 33 have been amended to recite “electrically separated.” As this change clearly involves no new examination or search issues, entry is believed to be in order.

This amendment is further believed to even more clearly highlight the difference in the electrical connection of the Yanagisawa emitter voltage sensing terminal to its main emitter and the “electrically separate” connection between the current sense emitter and main emitter of independent Claims 25, 27, 29, 31, and 33.

In this last regard, the requirement for an electrical connection between any of 12, 12a, and 38 of the IGBT 10 shown by FIGS. 6-8 of Yanagisawa is believed to be clear from the above discussion thereof. On the other hand, the electrical separation between the current sense emitter and the main emitter of the IEGT of the present invention is clear from a consideration of Application FIG. 24, for example, also discussed above as to showing the equivalent circuit of IEGT 42a. Support for the need for electrical separation between a current sense emitter and a main emitter even in an IGBT is shown by FIGS. 7.46, 7.49, and 7.50 from pages 179-180 of the “Power Semiconductor and Power IC Handbook,” (1996) that is attached hereto.

FIG. 7.46 shown main emitter and a current sense emitter. This equivalent circuit of an IGBT has a similar structure as the IEGT 42A. Further, an equivalent circuit of this IGBT is shown in FIG. 7.49 on page 180 in which the IGBT shown in FIG. 7.46 is divided into two IGBTs including a main IGBT having the main emitter and a current detection IGBT having the current sense emitter. Further, a practical sectional structure of the IGBT shown in FIG. 7.46 having two emitters as shown in FIG. 7.49 is shown in FIG. 7.50 on page 180.

As can be seen from FIG. 7.50, the main IGBT and the current sense IGBT are separately formed in the device substrate (n base layer). Thus, the main emitter formed in the main IGBT is separated from the current sense emitter formed in the current sense IGBT.

In other words, when it is intended to sense the current flowing in the main emitter of the IGBT (or IEGT), it is absolutely necessary to provide the current sense emitter separated from the main emitter. If the current sense emitter is connected to the main emitter, it is not

possible to sense correctly the current flowing through the main emitter because a part of the current which should be directed to the main emitter is shunted to the current sense emitter.

As has been previously noted, Takeda shows no more than an IEGT with a trench gate that has a multi-emitter structure for an over current limiting circuit.

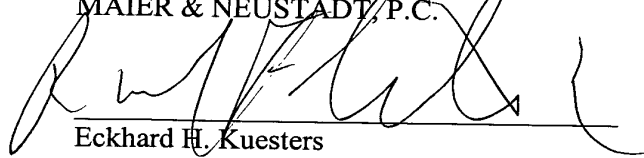
Therefore, it is again clear that Yanagisawa shows no more than a pressure-contact type IGBT having an emitter voltage sensing terminal connected to a main emitter and that Takeda shows no more than an IEGT having a double-emitter structure and does not show a pressure-contact type IEGT having a current sense emitter. Accordingly, even if the structure taught by Yanagisawa were to be modified by or combined with that shown by Takeda, the pressure-contact type IEGT having a current sense emitter electrically separate from the main emitter as recited in the amended independent claims is not the result and no *prima facie* case of obviousness has been established as to the subject matter of Claims 25-33.

Turning to the rejection of Claim 34 under 35 U.S.C. § 103(a) as being unpatentable over Yanagisawa in view of Takeda in further view of Horiguchi, it is again noted that Horiguchi cures none of the deficiencies noted above as to Yanagisawa and Takeda. In this regard, Horiguchi only teaches a transistor 5 and a resistor 7 connected to the gate of the transistor 5, see FIG. 1. However, the gate of the transistor 5 is not connected to receive a current extracted from a current sense emitter unlike the present invention recited in Claim 34. Therefore, the subject matter recited in Claim 34 is not obvious over Yanagisawa in view of Takeda and further in view of Horiguchi.

As no further issues are believed to remain outstanding in the present application, it is respectfully submitted that the present application is clearly in condition for formal allowance. Accordingly, an action to that effect is respectfully requested.

Respectfully submitted,

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Power Device · Power IC Handbook

パワーデバイス・ パワー IC ハンドブック

電気学会 高性能高機能パワーデバイス・パワー IC 調査専門委員会 編

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パワーデバイス・パワー IC ハンドブック
Power Semiconductor Device and Power IC Handbook

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1996 年 7 月 30 日 初版第 1 刷発行

検印省略

編 者 社団法人 電 気 学 会
高性能高機能パワーデバイス・
パワー IC 調査専門委員会

発 行 者 株式会社 コロナ社
代 表 者 牛来辰巳

印 刷 所 新日本印刷株式会社

112 東京都文京区千石 4-46-10

発行所 株式会社 コロナ社

CORONA PUBLISHING CO., LTD.

Tokyo Japan

振替 00140-8-14844・電話 (03) 3941-3131 (代)

ISBN 4-339-00653-X

(製本: 染野製本所)

Printed in Japan



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できる GTO のオフ時の破壊現象と類似の問題も潜在していると考えられる。

半導体素子が破壊に進行するメカニズムは、印加電圧が低い場合は温度上昇による電流増大の正帰還現象(熱暴走)がトリガであると考えられる。数十 V 以下でラッチアップ動作させたり負荷短絡動作させた場合がこの状況にあたる。印加電圧が定格電圧の数割以上になると、破壊に進行するトリガはダイナミックアバランシ現象も無視できなくなる。この現象は、高電界領域中の電流を構成する電荷の存在が電界強度分布を偏在化させ、その結果できた高電界強度部分で電荷が増倍され、その電荷が電界強度分布をより偏在化させるといったプロセスで電流増大の正帰還プロセスが働き、温度上昇が起こる間もないごく短い時間内に破壊に至るものである。

半導体素子は、破壊を進行させる電流増大メカニズムを有するばかりでなく電流抑制メカニズムも有しており、特定の電流、電圧でバランスが崩れ、前者が優勢になったときに破壊すると一般的に考えることが妥当である。例えば、IGBT は負荷短絡動作状態にあってもチップ内に均一な電流が流れている⁵⁴⁾ことは、電流抑制メカニズムの内在なくしては考えられない。このような観点からの破壊現象の解析は、バイポーラトランジスタの例⁵⁵⁾はあるが IGBT ではいまだ行われていない。

IGBT の破壊メカニズムは、デバイスシミュレーションを活用して分析が行われているがいまだ十分でなく、高耐圧 IGBT の破壊現象の解析と高耐量化技術は現在のパワーデバイスの最も興味ある技術分野の一つである。

7.3.6 高機能化技術

IGBT は、単純なスイッチングデバイスとして開発が進められたが、特性改善もほぼ理論限界値に達するまでになりつつある。そのつぎのデバイスとして、さらに機能を追加させることにより使いやすさを追求している。

過電流保護機能を内蔵し、IGBT としての特性を向上させる試みがなされている⁶¹⁾。図 7.46 にその基本構成を示す。IGBT に過電流が流れると、その電流をセンシングして制御回路に送り、ゲート電圧を制限して電流を抑制するものである。IGBT では、短絡耐量と損失の関係はトレードオフの関係にあり、短絡耐量を増加させると素子損失は大きくなる。この過電流制限機能を付加した IGBT は、このトレードオフの関係をブレークスルーしたもので、素子損失の改善を図りながら、短絡時の過電流は制限回路にて対処しようとしたもの

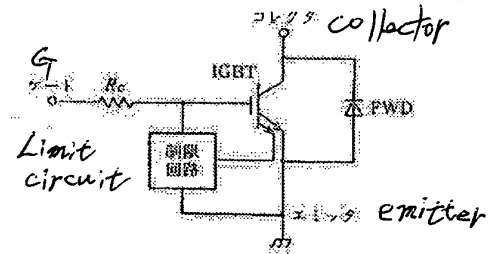


図 7.46 過電流制限回路

Over-current limiting ckt

である。

さらに過電流制限回路を IGBT に内蔵しようとする試みがなされている^{58), 59)}。

2 社から同様の報告がなされているが、ここにそれぞれの等価回路および断面構造図を示す。

図 7.47、図 7.48 は図 7.46 により報告されているものである。その構成は、センシング IGBT、横形 MOSFET、多結晶シリコンダイオードなどから構成されている。実際に作成した素子では、十分な過電流制限がなされ、素子の損失も低減されたと報告されている。

図 7.49、図 7.50 は清水らにより報告されているもの

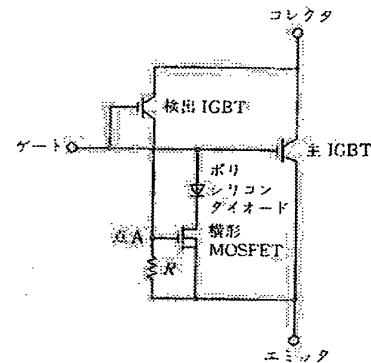


図 7.47 過電流制限回路を内蔵している IGBT の等価回路

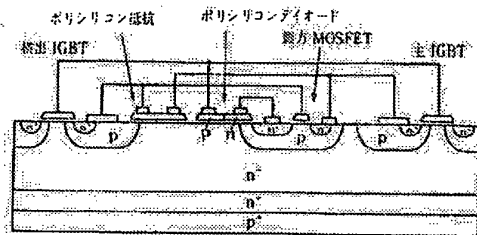


図 7.48 新しい IGBT の断面図

で、ツェナーダイオードが用いられているのが特徴である。これも十分な短絡耐量が得られたと報告されている。

現状ではまだ、これらのように過電流制限回路を1チップ化したものは、市場に供給されるまでには至っていない。

過電圧保護回路を内蔵した IGBT の報告が山崎らによってなされている⁵⁰⁾。これは IGBT の表面に IGBT の耐圧よりわずかに低いアバランシダイオードを形成し、過電圧が IGBT に印加されるところのダイオードが先にアバランシ状態に入り、ゲートをオンさせて、主 IGBT を過電圧から保護するものである。断面構造および等価回路を図 7.51、図 7.52 に示した。この過電圧保護回路の内蔵により、素子の損失を 25% 低減すること

ができたと報告している。

過熱感知についても、IGBT に組み入れた報告が岩室らにより報告されている⁵¹⁾。その断面構造を図 7.53 に示す。これは素子の表面に酸化膜を介して多結晶シリコンのダイオードを形成し、その順電圧の変化を温度として検出しているものである。

従来は IGBT デバイスそのものではなく、基盤を介してサーミスタなどで温度を測定していたが、この方式では直接 IGBT チップの温度を検知できるため、精度の高い温度検知が可能である。実際の温度検知の様子を図 7.54 に示した。ここでは、短絡時に素子の温度が上昇している様子が示されている。

7.3.7 pチャネルデバイス

pチャネル IGBT は、nチャネル IGBT と組み合わせ

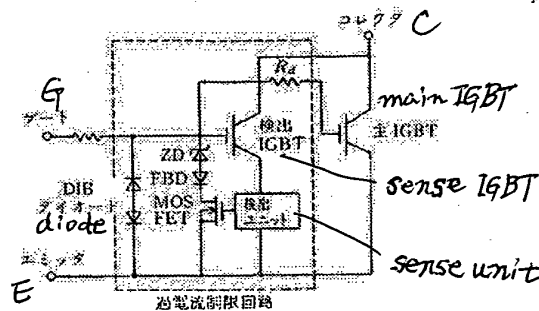


図 7.49 過電流制限機能をもつ IGBT

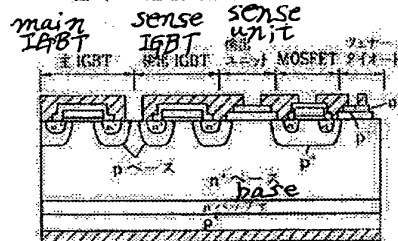


図 7.50 デバイスの断面概略図

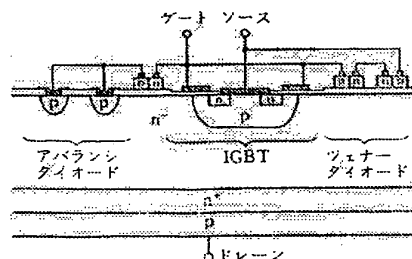


図 7.51 過電圧保護回路をもつ IGBT の断面図

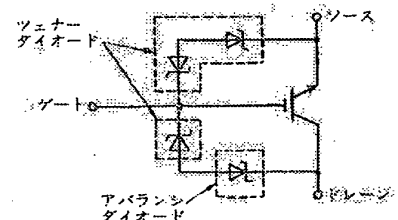


図 7.52 デバイスの等価回路

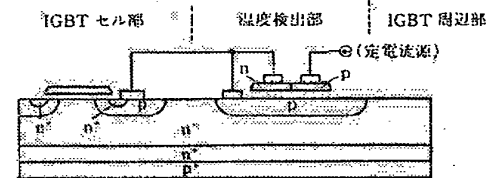


図 7.53 新形 IGBT 断面構造図

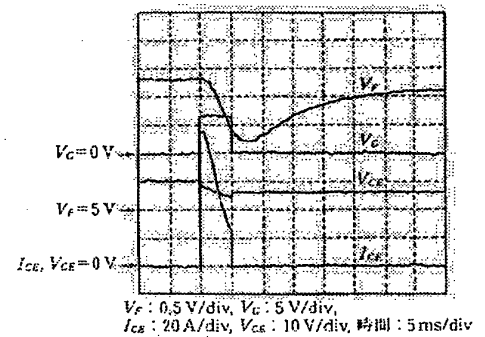


図 7.54 IGBT 負荷短絡時の波形

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